Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-2. (Canceled)

3. (Currently Amended) A microprocessor comprising:

a memory array having a stack for saving contextual data; and

a central processing unit coupled to the memory array, the central processing unit having registers containing contextual data and a stack pointer and being arranged for saving contextual data upon a switch from a first to a second program in a variable number of registers that varies according to a value of at least one flag stored in a register to be saved,

wherein the central processing unit is arranged for changing the value of the at least one flag according to the content of an extended addressing register of a program counter of the central processing unit before saving contextual data contained in a variable number of registers that varies according to the value of the at least one flag, wherein the central processing unit is arranged for, when the content of the extended addressing register is equal to a first value, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register.

4. (Currently Amended) The microprocessor according to claim 3 wherein the central processing unit is arranged for:

~~when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register; and~~

when the content of the extended addressing register is not equal to ~~0~~ the first value, saving all the registers of the central processing unit containing contextual data, including the extended addressing register.

5. (Previously Presented) The microprocessor according to claim 3 wherein the central processing unit is arranged for performing a test on the value of the at least one flag so as to determine the number of registers to be saved.

6. (Previously Presented) The microprocessor according to claim 3 wherein the central processing unit is arranged for, upon the return to the first program:

restoring the register containing the at least one flag at a first time; and

restoring contextual data contained in a variable number of registers that varies according to the value of the at least one flag present in the restored register at a second time subsequent to the first time.

7. (Previously Presented) The microprocessor according to claim 3 wherein the central processing unit is arranged for saving the register containing the at least one flag last.

8. (Previously Presented) The microprocessor according to claim 3 wherein the at least one flag comprises at least one bit of a register containing condition code flags.

9-10. (Canceled)

11. (Currently Amended) A method for managing a stack of a microprocessor having a central processing unit and a memory array, the central processing unit having registers containing contextual data and a stack pointer, the stack being a zone of the memory array dedicated to saving contextual data upon a switch from a first to a second program, the method comprising:

saving contextual data contained in a variable number of registers that varies according to the value of at least one flag stored in a register to be saved; ~~and~~

changing the value of the at least one flag according to the content of an extended addressing register of a program counter of the central processing unit before saving the contextual data; and

when the content of the extended addressing register is equal to a first value, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register.

12. (Currently Amended) The method according to claim 11, comprising the following steps:

~~when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register; and~~

when the content of the extended addressing register is not equal to ~~0~~ the first value, saving all the registers of the central processing unit containing contextual data, including the extended addressing register.

13. (Previously Presented) The method according to claim 11, comprising a step of:

testing the value of the at least one flag for determining the number of registers containing the data to be saved.

14. (Previously Presented) The method according to claim 11, comprising the following steps:

restoring the register containing the at least one flag; then

restoring contextual data contained in the variable number of registers that varies according to the value of the at least one flag present in the restored register.

15. (Previously Presented) The method according to one claim 11 wherein the register containing the at least one flag is saved last and is restored first.

16. (Previously Presented) The method according to claim 11 wherein the at least one flag is formed by at least one bit of a register containing condition code flags.

17. (Currently Amended) A microprocessor comprising:

a memory array having stored therein contextual data;

a central processing unit coupled to the memory array;

a plurality of registers associated with the central processing unit, a first group of the registers storing contextual data and a second group of the registers not storing contextual data when a flag has a first value and switching to store contextual data also in the second group of registers when the flag switches to a second value, such that the number of registers that store contextual data is variable,

and where the flag is stored in a register to be saved as part of the program contextual data ~~and where the flag is asserted when an extended portion of a program counter has a portion of an extended address~~;

a stack pointer associated with the central processing unit and being arranged for directing contextual data to be stored in the first group only or in both the second group and the first group, based on the flag value; and.

wherein the central processing unit is arranged for, when the content of the flag is equal to the first value, saving all the registers of the central processing unit containing contextual data, except for an extended addressing register.

18. (Original) The microprocessor according to claim 17 wherein the second group of registers includes a register which is used as an extended addressing register when the flag is at a first value.

19. (Original) The microprocessor according to claim 17 wherein the second group of registers includes a single register.

20-30. (Canceled)

31. (New) The microprocessor of claim 17 wherein the flag is asserted to the second value when the extended portion of the program counter has a portion of an extended address.